

WHAT IS CLAIMED IS:

- 1 1. A method for regenerating clock signals, comprising:
2 converting clock signals having either single- ended clock pulses or differential
3 clock pulses into clock signals having substantially the same voltage swing.
- 1 2. The method recited in claim 1 wherein the single-ended clock pulses are provided by a
2 TTL logic circuit and wherein the differential clock pulses are produced by an ECL logic
3 circuit.
- 1 3. A method for regenerating clock signals, comprising:
2 providing a source of clock signals, such source producing either single- ended
3 clock pulses or differential clock pulses, such clock signals being fed to a regeneration
4 circuit, such regeneration circuit converting such clock signals having either the single-
5 ended clock pulses or the differential clock pulses into clock signals having substantially
6 the same voltage swing.
- 1 4. A clock regeneration circuit, comprising:
2 a differential amplifier having a non-inverting input terminal and an inverting
3 input terminal;
4 a first voltage divider network coupled between a pair of reference voltages and
5 the non-inverting input terminal;
6 a second voltage divider network coupled between the pair of reference voltages
7 and the inverting input terminal;
8 wherein the first and second voltage divider networks produce the same voltage at
9 the inverting and non-inverting input terminals.
- 1 5. The clock regeneration circuit recited in claim 4 wherein the first voltage divider
2 network includes a pair of resistors, a first one of the pair of resistors, R1, being
3 connected between a first one of the pair of reference voltages and the non-inverting
4 input and a second one of the pair of resistors, R2, being connected between the non-
5 inverting input and the second one of the pair of reference voltages.

1 6. The clock regeneration circuit recited in claim 5 wherein the second voltage divider
2 network includes a pair of resistors, a first one of the pair of resistors, R3, being
3 connected between a first one of the pair of reference voltages and the inverting input and
4 a second one of the pair of resistors, R4, being connected between the inverting input and
5 the second one of the pair of reference voltages.

1 7. The clock regeneration circuit recited in claim 6 wherein R1 is has the same resistance
2 as R3 and R2 has the same resistance as resistor R4.

1 8. The clock regeneration circuit recited in claim 7 including a transmission line coupled
2 between a source of clock signals and the input terminals, and wherein such transmission
3 line has a characteristic impedance Z_o , and wherein $R1 \cdot R2 / (R1 + R2)$ equals Z_o .

1 9. The clock regeneration circuit recited in claim 8 wherein the source of clock pulses is
2 an emitter coupled logic circuit and wherein the potential difference provided by the pair
3 of reference voltages voltage, V_{cc} , times $(R2 / (R1 + R2))$ and V_{cc} , times $(R3 / (R3 + R4))$ are
4 selected to provide predetermined proper terminating voltages to the emitter coupled
5 logic circuit.

1 10. The clock regeneration circuit recited in claim 8 wherein the source of clock pulses is
2 a transistor-transistor logic circuit having an output transistor, such output transistor
3 having an emitter and collector coupled between the pair of reference potentials, and
4 including a coupling resistor R5 serially connected between the collector electrode and
5 the non-inverting input though the transmission line, such resistor R5 being selected to
6 provide a predetermined proper voltage swing across the non-inverting and inverting
7 inputs

1 11. A method for regenerating clock signals, comprising:
2 providing a source of clock signals, such source having either TTL logic circuit for
3 producing single- ended lock pulses or ECL logic circuit for producing differential clock
4 pulses,

5 providing a clock pulse regeneration circuit;
6 feeding to clock signals to the regeneration circuit, such regeneration circuit
7 converting such clock signals having either the single-ended clock pulses or the differential
8 clock pulses into clock signals having substantially the same voltage swing;
9 providing such regeneration circuit with:
10 a differential amplifier having a non-inverting input terminal and an
11 inverting input terminal;
12 a first voltage divider network coupled between a pair of reference
13 voltages and the non-inverting input terminal;
14 a second voltage divider network coupled between the pair of reference
15 voltages and the inverting input terminal;
16 wherein the first and second voltage divider networks produce the same
17 voltage at the inverting and non-inverting input terminals.

1 12. The method recited in claim 11 wherein the regeneration circuit the first voltage
2 divider network is provided with a pair of resistors, a first one of the pair of resistors, R1,
3 being connected between a first one of the pair of reference voltages and the non-
4 inverting input and a second one of the pair of resistors, R2, being connected between the
5 non-inverting input and the second one of the pair of reference voltages.

1 13. The method recited in claim 12 wherein the second voltage divider network is
2 provided with a pair of resistors, a first one of the pair of resistors, R3, being connected
3 between a first one of the pair of reference voltages and the inverting input and a second
4 one of the pair of resistors, R4, being connected between the inverting input and the
5 second one of the pair of reference voltages.

1 14. The method recited in claim 13 wherein R1 is has the same resistance as R3 and R2
2 has the same resistance as resistor R4.

1 15. The method recited in claim 14 including providing a transmission line coupled
2 between a source of clock signals and the input terminals, and wherein such transmission
3 line has a characteristic impedance Z_o , and wherein $R_1 * R_2 / (R_1 + R_2)$ equals Z_o .

1 16. The method recited in claim 15 including connecting to the transmission line either:
2 an emitter coupled logic circuit for producing the clock pulses and wherein the
3 potential difference provided by the pair of reference voltages voltage, V_{cc} , times
4 $(R_2 / (R_1 + R_2))$ and V_{cc} , times $(R_3 / (R_3 + R_4))$ are selected to provide predetermined proper
5 terminating voltages to the emitter coupled logic circuit; or
6 an transistor-transistor logic circuit for producing the clock pulses having an
7 output transistor, such output transistor having an emitter and collector coupled between
8 the pair of reference potentials, and including a coupling resistor R_5 serially connected
9 between the collector electrode and the non-inverting input through the transmission line,
10 such resistor R_5 being selected to provide a predetermined proper voltage swing across
11 the non-inverting and inverting inputs